FIG. 1

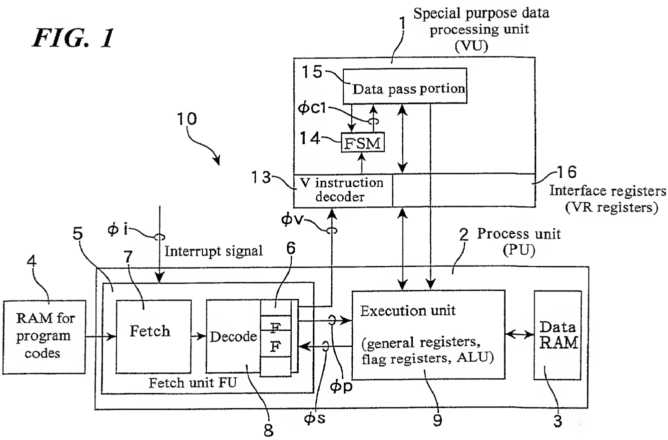

1
Special purpose data processing unit (VU)
15
Data pass portion
φc1
14
FSM
10
13
V instruction decoder
16
Interface registers (VR registers)
φv
φi
Interrupt signal
5
4
7
6
2 Process unit (PU)
RAM for program codes
Fetch
Decode
F
F
Execution unit
(general registers, flag registers, ALU)
Data RAM
Fetch unit FU
φp
φs
8
9
3

FIG. 2

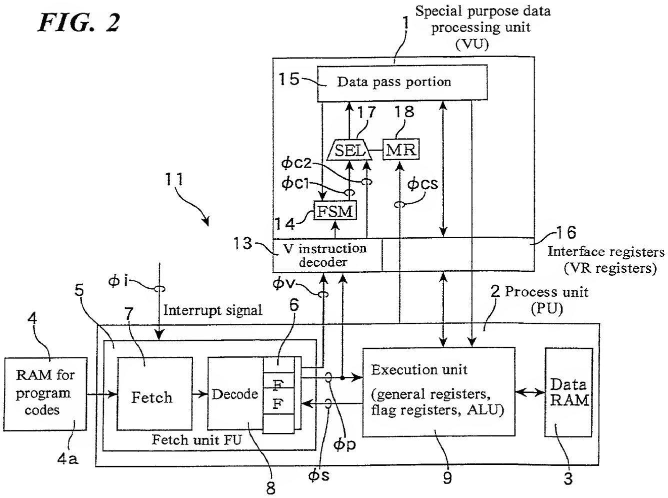

Special purpose data processing unit (VU)
1
15
Data pass portion
17
18
SEL
MR
φc2
φc1
φcs
FSM
14
11
13
V instruction decoder
16
Interface registers (VR registers)
φi
φv
5
Interrupt signal
6
2 Process unit (PU)
4
7
RAM for program codes
Fetch
Decode
F
F
Execution unit
(general registers, flag registers, ALU)
Data RAM
Fetch unit FU
φp
4a
φs
8
9
3

FIG. 3

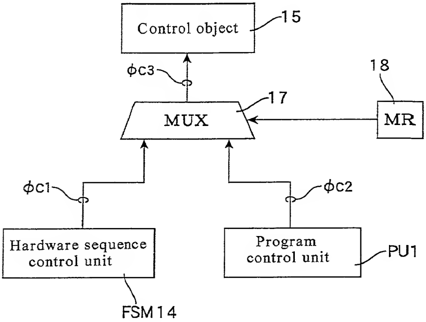

Control object
15
ϕc3
18
17
MUX
MR
ϕc1
ϕc2
Hardware sequence control unit
Program control unit
PU1
FSM14

FIG. 4

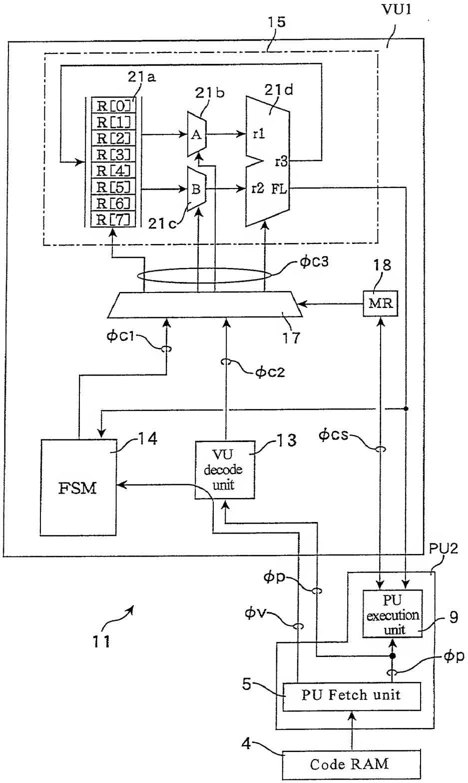
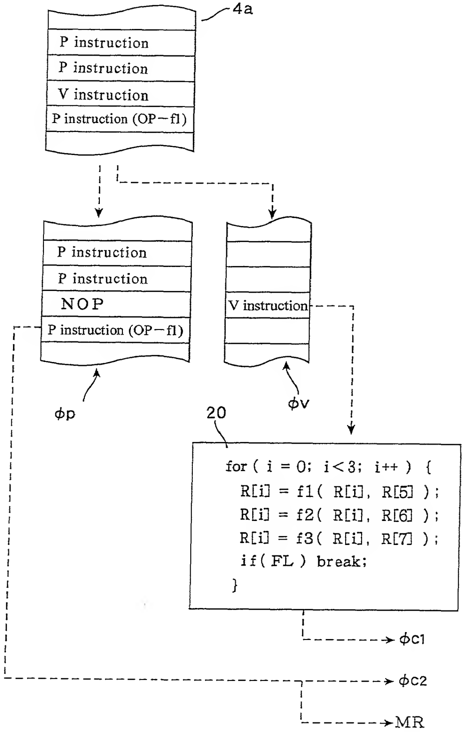

VU1
15
21a
21b
21d
R[0]
R[1]
R[2]
R[3]
R[4]
R[5]
R[6]
R[7]
A
B
r1
r3
r2
FL
21c
ϕc3
18
MR
17
ϕc1
ϕc2
14
FSM
13
VU decode unit
ϕcs
PU2
ϕp
PU execution unit
9
ϕv
11
ϕp
5
PU Fetch unit
4
Code RAM

FIG. 5



```
for ( i = 0; i<3; i++ ) {
  R[i] = f1( R[i], R[5] );
  R[i] = f2( R[i], R[6] );
  R[i] = f3( R[i], R[7] );
  if( FL ) break;
}
```

FIG. 6

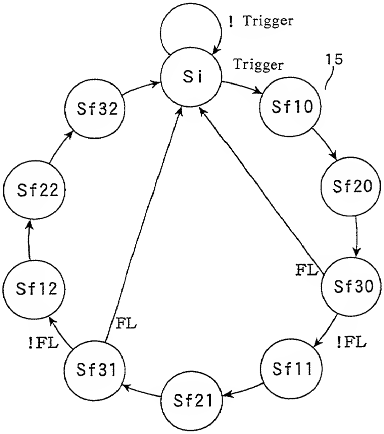

! Trigger
Trigger
15
Si
Sf10
Sf20
Sf30
Sf11
Sf21
Sf31
Sf12
Sf22
Sf32
FL
FL
!FL
!FL

FIG. 7

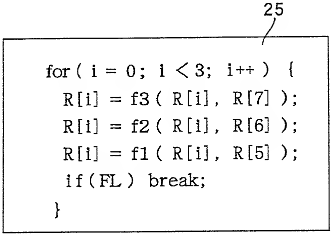
$\phi c1$

Status	Register file read out selection A	Register file read out selection B	Calculation selection	Register file write selection・approve
Si	no read out	no read out	no calculation selection	no write
Sf10	R[0]	R[5]	f1	R[0]
Sf20	R[0]	R[6]	f2	R[0]
Sf30	R[0]	R[7]	f3	R[0]
Sf11	R[1]	R[5]	f1	R[1]
Sf21	R[1]	R[6]	f2	R[1]
Sf31	R[1]	R[7]	f3	R[1]
Sf12	R[2]	R[5]	f1	R[2]
Sf22	R[2]	R[6]	f2	R[2]
Sf32	R[2]	R[7]	f3	R[2]

FIG. 8

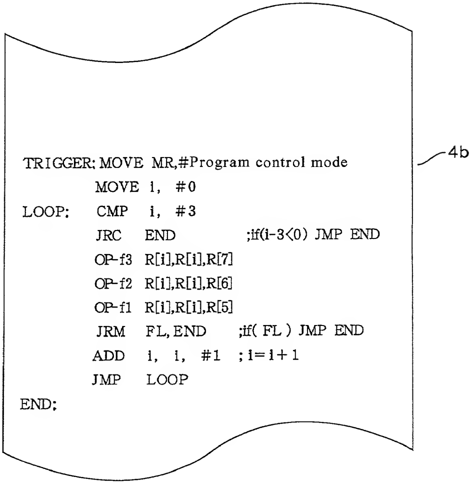
	ϕc2			
Instruction	Register file read out selection A	Register file read out selection B	Calculation selection	Register file write selection・approve
OP−f1 r3, r1, r2	r1	r2	f1	r3
OP−f2 r3, r1, r2	r1	r2	f2	r3
OP−f3 r3, r1, r2	r1	r2	f3	r3

FIG. 9



```
for ( i = 0;  i < 3;  i++ )  {
  R[i] = f3 ( R[i], R[7] );
  R[i] = f2 ( R[i], R[6] );
  R[i] = f1 ( R[i], R[5] );
  if (FL )  break;
}
```

FIG. 10



```
TRIGGER: MOVE  MR,#Program control mode
         MOVE  i,  #0
LOOP:    CMP   i,  #3
         JRC   END           ;if(i-3<0) JMP END
         OP-f3 R[i],R[i],R[7]
         OP-f2 R[i],R[i],R[6]
         OP-f1 R[i],R[i],R[5]
         JRM   FL,END       ;if( FL ) JMP END
         ADD   i,  i,  #1   ;i=i+1
         JMP   LOOP
END:
```

FIG. 11

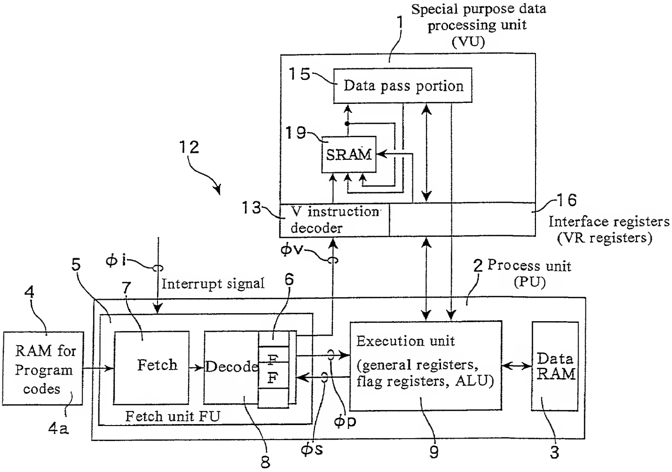
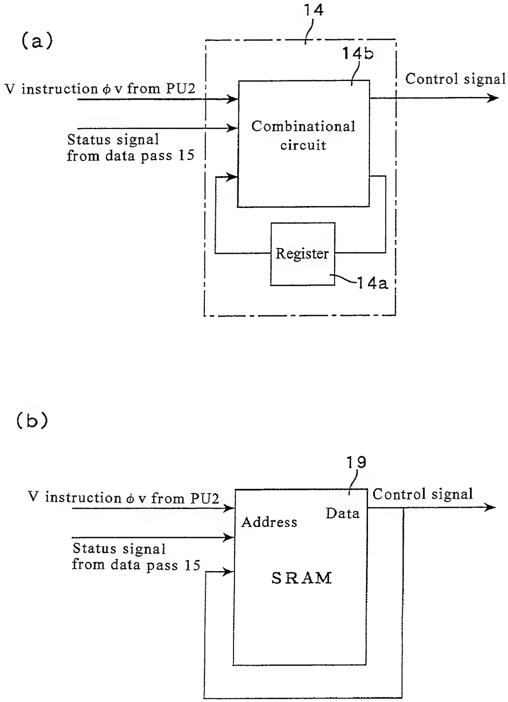

Special purpose data processing unit (VU)
1
15
Data pass portion
19
SRAM
12
13
V instruction decoder
16
Interface registers (VR registers)
φv
φi
Interrupt signal
5
4
7
6
2 Process unit (PU)
RAM for Program codes
4a
Fetch
Decode
F
F
Fetch unit FU
Execution unit
(general registers, flag registers, ALU)
Data RAM
φp
φs
8
9
3

FIG. 12


(a)
14
14b
V instruction ϕ v from PU2
Status signal
from data pass 15
Combinational
circuit
Control signal
Register
14a
(b)
19
V instruction ϕ v from PU2
Status signal
from data pass 15
Address
Data
SRAM
Control signal